REMARKS

Claims 1-12 remain pending in the application. Claims 2 and 3 have been amended without introduction of new matter. Favorable reconsideration is respectfully requested in view of the above amendments and the following remarks.

Claims 2 and 3 were rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite. It is believed this rejection is overcome by the foregoing amendment. More specifically, claims 2 and 3 have been amended to indicate that the length of the bus portions refers to a physical length. Support for this amendment may be found, for example, in the specification at page 30.

Claims 1, 2, 3, 5, and 12 stand rejected under 35 U.S.C. §102 (b) as allegedly being anticipated by Japanese Patent Number JP 08147163 ("Takemoto"). This rejection is respectfully traversed.

Based on the available English language abstract and Figure 1, Takemoto appears to disclose a pipeline comprising processors 13, 14 that are adapted to perform prescribed instruction processing operations in respective stages of the pipeline. The data to be processed is held in registers 15, 17, 19. Multiplexers 16, 18 and 20 are illustrated as being connected between the registers and the respective processors and are connected to a control device 21. However, the processors are not connected to the bus stages through the multiplexers. The function of the processors seems to be to provide a direct signal path from the preceding register or a by-pass path, depending on instruction from the controller 21. This approach would be consistent with Takemoto in addressing stalling in the pipeline.

Takemoto fails to disclose Applicant's invention as recited in claim 1. In particular, Takemoto fails to disclose a bus architecture in which bus connection units connect bus portions together in series. Takemoto also fails to disclose each of the modules (i.e. the processors 13, 14) being connected to the bus architecture by way of a respective bus

connection unit. Furthermore, Takemoto also fails to disclose multiplexer circuitry for selectively connecting a module to the bus architecture.

Takemoto, therefore, fails to anticipate Applicant's invention as recited in claim 1.

Claims1, 2, 3, 5 and 12 also stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by US Patent No 5,325,495 ("McLellan"). This rejection is also respectfully traversed.

McLellan, in Figure 1, illustrates a pipeline architecture comprising a number of pipeline stages having successive "operational stages" (i.e. modules) 10, 11, 12 and 13 and instruction stages #1, #2, #3 and #4 connected to a pipeline control device 20 and to respective operational stages. Additional Q-stages are inserted in the pipeline to prevent stalling. The Q-stage comprises a through path and a queue path containing a Q device 16. A multiplexer 18 passes data from the upstream stages to the downstream stages via the through path or the Q-path under instruction from the controller 20.

The multiplexer configuration in McLellan is similar to that disclosed in Takemoto. It (i.e. the multiplexer configuration of McLellan) is not used for selectively connecting a module to the bus architecture. The modules are permanently connected to the bus architecture in McLellan and the multiplexers serve a completely different purpose and function, namely providing a choice of data path from one bus portion/stage to the next. The multiplexers do not selectively connect a module to the bus architecture. In addition, Figure 1 does not disclose each bus portion (except the last) being connected to the next portion in series by way of a bus connection unit. McLellan is concerned with the problem of avoiding stalling and is not concerned with a modular arrangement where modules can be connected into a bus architecture having a plurality of modules connected in series via bus connection units, each of which (bus connection units) includes multiplexer circuitry for selectively connecting a module to the bus architecture.

McLellan also fails to anticipate Applicant's invention as recited in claim 1.

Claims 1, 2, 3, 5 and 12 also stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by US Patent No 5,555,384 ("Roberts"). This rejection is also respectfully traversed.

Roberts, in Figure 6, illustrates a floating point coprocessor (FPC) forming part of a method and apparatus for optimising the operation of an instruction pipeline in a computer so as to reduce stalling. Roberts is directed to "pipelining" (col. 1, lines 27-35) which is a technique described as involving the overlapping of instruction streams. Roberts is not concerned with a particular form of bus architecture as in Applicant's invention. As in Takemoto and McLellan, Roberts describes a bypass technique (col. 5, lines 31-51) where a set of bypass multiplexers are used to couple the various stages (registers 33, 35, 37) together. Switching the data paths by means of the multiplexers, under control of device 50, reduces the length of a pipeline stall.

Roberts merely describes the use of multiplexers to alter the path between nodes along the pipeline. If the registers 33, 35, 37 of Roberts are to be treated as the modules of Applicant's invention recited in claim 1, Roberts fails to disclose each of the bus connection units including multiplexer circuitry for selectively connecting a module to the bus architecture. The multiplexers of Roberts not only fail to perform this function; they are also not connected into the bus structure in the manner necessary to enable a module to be selectively connected to the bus structure.

Roberts also fails to anticipate Applicant's invention as recited in claim 1.

Each of Takemoto, McLellan and Roberts fails to disclose an apparatus in which each bus connection unit includes a multiplexer (or multiplexer circuitry) for selectively connecting a module to the bus architecture. It is important to recognize the technical significance of the emphasized wording in the context of Applicant's bus architecture. The

multiplexers in each of the cited patents perform different functions to those in Applicant's invention. The modules/units in the cited patents are permanently incorporated into the respective bus architectures while the multiplexers are used as switches to effect bypass switching so as to reduce stalling.

In Applicant's invention (Specification, page 30), each of the bus connection units has in-built buffering and output circuitry tailored to the length of the bus between it (i.e. bus connection unit) and the next node. This enables a node to be omitted while maintaining bus characteristics (i.e. selectively connecting). This feature is not contemplated in any of Takemoto, McLellan or Roberts as they fail to disclose the underlying architecture to make use of this feature. Furthermore, the bus connection units in Applicant's invention are the means by which each module is connected to the pipeline bus. The modules in Applicant's invention are not "in-line" with the pipeline bus but are coupled to it "sideways" through the bus connection units. This is illustrated in Figure 30 of Applicant's invention.

For at least the foregoing reasons, Applicant respectfully submits that claim 1 is allowable over the teachings of each of Takemoto, McLellan and Roberts. Claims 2, 3, 5 and 12, all of which depend on claim 1 are also allowable.

Claims 4, 6, 7 and 8 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Takemoto as applied to claims 1 and 5 and further in view of US Patent No 5,627,976 ("McFarland"). Claims 9 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Takemoto as applied to claim 1 and further in view of US Patent No 5,128,926 ("Perlman"). Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Takemoto as applied to claim 1 and further in view of US Patent No 5,925,118 ("Revilla").

In view of the arguments set forth above in support of Applicant's earnest contention that claims 1, 5 and 12 are novel over each of Takemoto, McLellan and Roberts, it is

In view of the arguments set forth above in support of Applicant's earnest contention that claims 1, 5 and 12 are novel over each of Takemoto, McLellan and Roberts, it is respectfully submitted that the further rejections relating to the alleged obviousness of claims 4 and 6-8 in view of McFarland, the alleged obviousness of claim 9 in view of Perlman and the alleged obviousness of claims 10 and 11 in view of Revilla are all now moot and require no specific attention in this response. It is accordingly respectfully requested that the rejections of claims 4 and 6-11 under 35 U.S.C. §103(a) be withdrawn.

The application is believed to be in condition for allowance. Prompt notice of same is respectfully requested.

Respectfully submitted,
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Date: June 9, 2006

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